

## Problem 3: Flip Flop Counters (10 points) [File Upload]

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## **Problem Statement**

Design a hardware counter that counts the following three bit sequence out of single bit D flip flops and JK flip flops

000, 010, 101, 111, 101, 010, 000, 010, 101, ...

**D** Flip Flops and State Transition Diagrams A D flip-flop is a basic digital circuit element that stores a single bit (0 or 1). It has a "Data" input *D* where you input the bit to be stored, and it updates its state in the next clock cycle after the clock signal toggles. The D flip-flop outputs the stored bit *Q*.

State transition diagram represents the transitions between different states of a system. Each line represents a state and a transition to a next state depending on its current state and inputs, providing a concise depiction of the system's behavior over time. Below is the state transition diagram for a D flip flop.

Table 1: D Flip-Flop State Transition Diagram

Current State $(Q(t))$	Input $(D(t))$	Next State $(Q(t+1))$
0	0	0
0	1	1
1	0	0
1	1	1

Boolean Functions and Don't Cares: "Don't cares" refer to specific input combinations where the function's output is undefined or irrelevant. "Don't cares" provide flexibility in simplifying the logic expressions and can be used to design more efficient boolean functions. Use x or d to indicate don't cares in your state transition tables.





**Part 1:** Implement the desired counter using the minimal number of D flip flops and describe state transitions and inputs in the most reduced sum of products form boolean statements.

The counter should be designed as a Moore machine, such that the outputs only depend on the current state. You can assume that there are no inputs and that the state will transition each clock cycle.

For grading consistency, you can assume that the D flip flops will start from state 0 and output 000, and that the state numbers increment accordingly (*e.g.* state 1 outputs 010). Label the state D flip flops and outputs from left to right to be most significant bit n to least significant bit 0.

Derive the state transition table where each row has a current state, the next state it will transition to, and the output of the current state. The state transition table should only be 0, 1, or don't cares. Also provide the simplified sum of products boolean expression for each D flip flop's input D value to transition to the next state and each output based on the bit values of the current state.

Current State $(Q_n,, Q_0)$	Needed Input Values $(D_n,, D_0)$	<b>Output</b> $(O_2, O_1, O_0)$
0		000
1		010

Table 2: D Flip Flop Co	ounter Transition Diagram
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$D_n = F(Q_n, \dots Q_0)$	$O_2 = ?$
÷	$O_1 = ?$
$D_0 = ?$	$O_0 = ?$





**Part 2:** Implement the desired counter using JK flip flops. JK flip flops are digital circuit elements that have two inputs and have the following state transition table:

Current State $(Q(t))$	Input (J)	Input (K)	Next State $(Q(t+1))$
0	0	0	0
1	0	0	1
d	0	1	0
d	1	0	1
0	1	1	1
1	1	1	0

<b>T</b> 1 1 0	TT 7	<b>D11 D1</b>	a		<b>T</b> 1 1
Table 3:	JK	Flip-Flop	State	Transition	Table

The number of JK flip flops you will use will be the same as the number of D flip flops you used in part 1 as the states have not change.

Fill out the state transition table and determine the simplified sum of products boolean expression for each JK flip flop's inputs J K value to transition to the next state and each output based on the bit values of the current state.

Table 4:	JK Flip	Flop	$\operatorname{Counter}$	Transition	Diagram
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Current State $(Q_n,, Q_0)$	Needed Input Values $(J_n, K_nJ_0, K_0)$	Output $(O_2, O_1, O_0)$
0		000
1		010

$$J_{n} = F(Q_{n}, ...Q_{0})$$

$$K_{n} = ?$$

$$\vdots$$

$$J_{0} = ?$$

$$K_{0} = ?$$

$$O_{2} = ?$$

$$O_{1} = ?$$

$$O_{0} = ?$$





How to Submit: submit a single PDF titled according to the provided naming convention for both parts and clearly label which is part 1 and part 2. Within the file, please also include your team ID somewhere. You can hand write the problem if it will be legible, attach screenshots within the PDF, or use LATEX.

